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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 16

Application Number: 08/798,227
Filing Date: February 11, 1997
Appellant(s): KEETH, BRENT

Memory system with Dynamic Timing Connection
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed September 10, 1999.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1 through 6, 8 through 11, 13 through 18 and 20 through 24 which are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 5,577,236 to Johnson et al..

This appeal involves claims 7, 12 and 19 which are rejected under 35 U.S.C. 103(a) as being obvious over the patent US Patent number 5,577,236 to Johnson et al. in view of US Patent Number 5,020,023 to Smith.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is substantially correct. The brief incorrectly lists the claims rejected under 35 U.S.C. 102(e). The correct statement of issue in the brief are as follows: 1) whether the Examiner properly rejected claims, 1 through 6, 8 through 11, 13 through 18 and 20 through 24 under 35 U.S.C. 102(e) as

being anticipated by US Patent number 5,577,236 to Johnson et al.; and 2) whether the Examiner properly rejected claims 7, 12 and 19 under 35 U.S.C. 103(a) as being obvious over the patent US Patent number 5,577,236 to Johnson et al. in view of US Patent number 5,020,023 to Smith.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1 through 24 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,577,236	Johnson et al.	12-1994
5,020,023	Smith	5-1991

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 through 6, 8 through 11, 13 through 18 and 20 through 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent number 5,77,236}. This rejection is set forth in prior Office Action, Paper No. 11.

With respect to claim 1, Johnson discloses a method for adjusting data timing in a memory system having a memory device and a memory controller. This is taught as synchronize the receipt by a latch **322**, memory bank **300**, from the memory bank **300** and the memory controller, at column 6 lines 8 to 18. "In particular, one of the sampling clock signals from the sampling clock circuit **304** is selectively fed to a delay module **313**, which provides a delayed clock signal to a first receiver **319** via an output line **317**, to synchronize the receipt by a latch **322** of Read data from the memory bank **300** during the appropriate data valid window." Johnson discloses the system operating according to a master clock signal. This is taught as provides signals resembling and system clock signal, at column 6 lines 19 to 46. "The sampling clock circuit **304** may comprise, for example, an oscillator that provides signals resembling the system clock signal." Johnson discloses transmitting a second set of data from the memory device to the memory controller according to the revised output timing. This is taught as compensating for data skew, appropriate data valid window, coordinate the receipt of data, read from the memory bank **300**, the memory controller and synchronize the receipt by a latch **322**, at column 6 lines 8 to 18. "The memory controller also includes a sampling clock circuit **304** to coordinate the receipt of data read from the memory bank **300** during the appropriate data valid window, thus compensating for data skew."

With respect to claims 1 and 20, Johnson discloses the method comprising the steps of establishing an initial output timing at the memory device, transmitting an echo clock [first digital] signal, receiving the echo clock [first digital] signal at the memory controller, identifying a phase error [difference], transmitting control data [adjustment signal], revising the initial output timing and transmitting a second set of data. This is taught as signal indicative of the level of memory loading, selectively directs an appropriate, signal lines **350** exhibit different phase characteristics, response to this signal, mux **307** to select one of the sampling clock signal and sampling clock signal on a line **352**, at column 6 lines 19 to 46. "The sampling clock signals on the signal lines **350** exhibit different phase characteristics (i.e. delays) with respect to each other, as described in greater detail below. The sampling clock signals are provided to a clock selector **306**, which selectively directs an appropriate one of the sampling clock signals to the delay module **313**." "The mux driver **312** receives a signal indicative of the level of memory loading, i.e. the number of memory modules **300*a*-300*d*** present. In response to this signal, the mux driver **312** provides an input signal on input lines **310** of the mux **307**, causing the mux **307** to select one of the sampling clock signal on a line **352** and provide an output signal comprising the selected sampling clock signals on a line **352**." Johnson discloses transmitting an echo clock [first digital] signal from the memory device to the memory controller according to the initial output timing. This is taught as receipt of data read, from the memory bank **300**, memory controller and signal indicative of the level of memory loading, at column 6 lines 8 to 46. Johnson discloses

identifying a phase error of the received echo clock [first digital] signal relative to the master clock [timing reference] signal. This is taught as provide an output signal, signal lines **350** exhibit different phase characteristics and selected sampling clock signals on a line **352**, at column 6 lines 19 to 46. Johnson discloses transmitting control data [adjustment signal] from the memory controller to the memory device for revising the initial output timing in response to the identified phase error [difference] to produce a revised output timing. This is taught as progressively greater and/or lesser delays, memory controller, memory modules **300*a*-300*d***, signal indicative of the level of memory loading, selectively directs an appropriate one of the sampling clock signals, provide an output signal and chosen to exhibit the same timing characteristics, at column 6 lines 8 to 46. "As described in greater detail below, one of the sampling clock signal on a line **350** may be chosen to exhibit the same timing characteristics as the system clock signal on the signal line **348**, with the remaining clock signals of the lines **350** containing progressively greater and/or lesser delays of desired increments." Johnson discloses revising the initial output timing of the memory device according to the control data [adjustment signal]. This is taught as mux **307** to select one of the sampling clock signal, memory modules **300*a*-300*d*** and input lines **310** of the mux **307**, at column 6 lines 19 to 46. "The clock selector **306** includes a multiplexer **307** ('mux') and a multiplexer driver **312** ('mux driver')."

With respect to claims 2 and 21, Johnson discloses wherein the step of identifying a phase error of the received echo clock signal relative to the [timing

reference] master clock signal comprises the steps of generating a plurality of phase shifted signals, comparing the echo clock signal and identifying one of the phase shift signals. This is taught as correct sampling clock signal, the interval of delay, correct sampling clock signal, based upon data received, [provide repeating 10 nS], system clock signal, the sampling clock signals **400-403**, interval of delay between successive sampling clock signals **400-403**, interval of delay, based upon data received, sampling clock signals **400-403** and the interval of delay, at column 8 lines 1 to 32. "Thus the system clock signal and the sampling clock signals **400-403** provide repeating 10 nS 'on' periods, spaced apart by 10 nS 'off' periods." "The predetermined delay of each sampling clock signal **400-403** with respect to the system clock signal is preferably selected based upon the expected levels of memory loading, the interval of delay between successive sampling clock signals **400-403** are delayed, with respect to the system clock, by the following amounts." "Generally, the clock selector **306** selects one of these signals to forward to the delay module **313**, to coordinate timing of data Read operations with the memory bank **300**. More specifically, the mux driver **312** provides an output on the mux input lines **310**, causing the mux **307** to output the correct sampling clock signal on the signal line **352**. In an illustrative embodiment, the mux driver **312** provides its output based upon data received from a data source **305** via a selector bus **311**, in the manner discussed below." Johnson discloses generating a plurality of phase shifted signals responsive to the [timing reference] master clock signal, comparing the echo clock signal and identifying one of the phase shifted signals.

This is taught as the sampling clock signals **400-403**, [provide repeating 10 nS], system clock signal, based upon data received, coordinate timing of data Read and correct sampling clock signal, at column 8 lines 1 to 32. Johnson discloses comparing the echo clock signal to each of the phase shifted signals. This is taught as based upon data received and correct sampling clock signal, at column 8 lines 1 to 32. Johnson discloses identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal. This is taught as the clock selector **306** selects one of these signals, correct sampling clock signal and based upon data received, at column 8 lines 1 to 32.

With respect to claims 3 and 22, Johnson discloses wherein the step of establishing an initial output timing includes the steps of setting a delay of a delay circuit and applying a master clock signal to the delay circuit to produce the echo clock signal. This is taught as in accordance with the timing provided, the selection of the appropriate sampling clock signal, the delayed clock signal, system clock circuit **303**, delay module **313** and latch the READ data, at column 7 lines 21 to 40. "Specifically, in the act of reading data from the memory bank **300**, the appropriate module **300*a*-300*d*** places the read data onto the bus **320** in response to the Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the

receiver **319** to present the appropriate clock signal to the latch **322** to latch the READ data received from the memory modules **300***a*-**300***d*."

With respect to claims 4 and 23, Johnson discloses wherein the step of establishing an initial output timing further includes the steps of storing data in an output register, clocking the register with the echo clock signal, and outputting data from the register in response to the echo clock signal. This is taught as the selection of the appropriate sampling clock signal, delayed clock signal provided on the line **317**, LATCH **322**, bus **320**, LATCH **322**, TO LOGIC CIRCUITRY and latch the READ data, at figure 3 and column 7 lines 21 to 40.

With respect to claims 5 and 24, Johnson discloses wherein the step of revising the initial output timing includes the step of adjusting the delay of the delay circuit. This is taught as introduce a greater delay and delay module **313**, at column 9 lines 19 to 27. "With a larger data skew, for example, a clock signal on one of the signal lines **350** would be chosen to introduce a greater delay into the delay module **313**. After the memory modules **300***a*-**300***d* receive a Read command from the command bus **349**, the memory modules **300***a*-**300***d* place the requested data on the bus **320**. In an exemplary embodiment of the invention, the clock selector **306** chooses the clock signal **402** as a default if no other clock signal **400**-**401** or **403** is selected."

With respect to claim 6, Johnson discloses a method of controlling data flow in a memory system including a memory controller and a memory device. This is taught as coordinating the provision of READ commands, memory bank **300**, command driver **308**

and memory bank **300**, at column 5 line 48 through column 6 line 7. "The system clock circuit **303** is also connected to an inverter **324**, which is connected to a command driver **308** that serves to initiate operations in the memory bank **300** by coordinating the provision of READ commands to the memory bank **300**." Johnson discloses the method comprising the steps of generating a master clock signal, transmitting the master clock signal, issuing a first read command to the memory device, producing an echo signal at the memory device in response to the first read command, transmitting a first set of data, transmitting the echo signal at the memory controller, receiving the echo signal at the memory controller, comparing the received echo signal to the master clock signal, selecting an adjusted time delay, issuing a second read command to the memory device, reading a second set of data and transmitting the second set of data. This is taught as system clock circuit **303**, on a signal line **348**, clock READ commands, the Read command signal, memory bank **300**, Read data from the memory bank **300**, clock READ commands, system clock circuit **303**, Read data from the memory bank **300**, memory controller, Read data from the memory bank **300**, memory controller, Read data from the memory bank **300**, synchronize the receipt by a latch **322**, in accordance with timing provided, clock READ commands, memory bank **300**, Read data from the memory bank **300** and an output signal comprising the selected sampling clock signals, at column 5 line 48 through column 6 line 46. "The memory controller **302** contains a number of different components. First, a system clock circuit **303** is provided to clock READ commands unto the memory bank **300**. The system clock circuit **303**

provides a system clock signal on a signal line **348**, which is connected to a system clock driver **301**." "The command driver **308** preferably comprises a latch (not shown) electrically connected in series to a signal-boosting driver (not shown) so that the driver **308** provides an output of the Read command signal in accordance with timing provided by the system clock signal." Johnson discloses transmitting the master clock signal from the memory controller to the memory device. This is taught as on a signal line **348**, system clock circuit **303**, command driver **308** and to the memory bank **300**, at column 5 line 48 through column 6 line 7. Johnson discloses producing an echo signal at the memory device in response to the first read command. This is taught as receipt of data read from the memory bank **300**, the memory bank **300** and Read command signals, at column 5 line 48 through column 6 line 18. Johnson discloses the echo signal having a phase shift relative to the master clock signal. This is taught as of Read data from the memory bank **300**, sampling clock signals, different phase characteristics and system clock signal, at column 6 lines 8 to 46. Johnson discloses transmitting a first set of data to the memory controller with a time delay relative to the echo signal. This is taught as sampling clock circuit **304**, memory controller, compensating for data skew and data read from the memory bank **300**, at column 6 lines 8 to 18. "More specifically, the sampling clock circuit **304** generates multiple sampling clock signals on signal lines **350**, one signal of which is selectively directed to the delay module **313**." Johnson discloses selecting an adjusted time delay in response to the step of comparing the received echo signal to the master clock signal. This is taught as the

selection, the appropriate sampling clock signal, delays introduced by the delay module **313**, the READ data and timing provided by the system clock circuit **303**, at column 7 lines 21 to 40. Johnson discloses reading a second set of data in response to the second read command. This is taught as provision of READ commands and to clock READ commands, at column 5 line 48 through column 6 line 7. Johnson discloses transmitting to the memory controller the second set of data with the adjusted time delay. This is taught as memory controller **302**, system clock driver **301** and timing the internal operations, at column 5 line 48 through column 6 line 7.

With respect to claim 8, Johnson discloses wherein the step of comparing the received echo signal to the master clock signal includes the steps of producing a plurality of phase-shifted signals in response to the master clock signal and comparing the echo signal to each of the phase-shifted signals. This is taught as data read from the memory bank **300**, system clock signal, delayed clock signal, system clock signals, different phase characteristics, system clock signal, synchronize the receipt by a latch **322**, Read data from the memory bank **300** and delayed clock signal, at column 6 lines 8 to 46.

With respect to claim 9, Johnson discloses wherein the step of selecting an adjusted time delay includes the step of identifying one of the phase-shifted signals closest in phase to the echo clock signal. This is taught as the selection, the appropriate sampling clock signal, the selection, the appropriate sampling clock signal,

delays introduced by the delay module **313** and latch the READ data, at column 7 lines 21 to 40.

With respect to claim 10, Johnson discloses a memory controller for a memory system including a plurality of memory devices coupled to common clock and command busses, the memory devices producing echo signals in response to clock signals on the clock bus. This is taught as memory controller, memory bank **300**, system clock signal, bus **320**, memory bank **300**, signal line **348**, signal line **348** and signal line **348**, at figure 3 and column 6 lines 8 to 46. Johnson discloses the controller comprising a master clock source coupled to the clock bus, a phase comparing circuit, a logic circuit coupled to the phase comparing circuit and a control data circuit having a command output. This is taught as memory controller, system clock signal, signal line **348**, sampling clock circuit **304**, receipt by a latch **322**, select one of the sampling clock signal on a line **352**, receipt by a latch **322**, mux driver **312** and output line **317**, at column 6 lines 8 to 46. Johnson discloses a master clock source coupled to the clock bus operative to produce a master clock signal. This is taught as SYSTEM CLOCK CIRCUIT **303**, signal line **348** and system clock signal, at figure 3 and column 6 lines 19 to 46. Johnson discloses a phase comparing circuit coupled to the clock bus and responsive to produce a phase signal in response to a phase difference between the echo signal and the master clock signal. This is taught as to the latch **322**, timing provided by the system clock circuit **303**, delayed clock signal provided on the line **317**, delayed clock signal, to latch the READ data and system clock circuit **303**, at column 7 lines 21 to 40. Johnson discloses

a logic circuit coupled to the phase comparing circuit and adapted to produce adjustment data in response to the phase signal. This is taught as multiplexer driver **312**, different phase characteristics, causing the mux **307**, provide an output signal and selected sampling clock signals, at column 6 lines 19 to 46. Johnson discloses a control data circuit having a command output coupled to the command bus and adapted to produce a command signal at the command output in response to the adjustment data. This is taught as memory controller **302**, command driver **308**, command bus **349**, receiving the Read command signals, conveyed to the memory bank **300** and accordance with timing provided, at column 5 line 48 through column 6 line 7. "The output of the command driver **308** is provided to the modules **300***a*-**300***d* via a command bus **349**."

With respect to claims 11 and 14, Johnson discloses wherein the phase comparator includes a signal source and a plurality of phase comparator. This is taught as DELAY MODULE **313**, LATCH **322**, SAMPLING CLOCK CIRCUIT **304** and signal lines **350**, at figure 3. Johnson discloses a source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal. This is taught as signal lines **350**, multiple sampling clock signals, exhibit different phase characteristics and system clock signal, at column 6 lines 19 to 46. Johnson discloses each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the clock bus to receive echo signals and a phase output coupled to the logic circuit. This is taught as clock selector

306, sampling clock signal 400-403, predetermined delay, with respect to the system clock signal, system clock signal, based upon data received, sampling clock signals 400-403 and mux 307, at column 8 lines 1 to 32.

With respect to claim 13, Johnson discloses a memory system, comprising a command bus, a clock bus, a data bus, a memory controller and a memory device. This is taught as memory bank 300, command bus 349, SYSTEM CLOCK 348, data source 305, via a selector bus 311, memory controller 302 and memory bank 300, at figure 3. Johnson discloses a memory controller including a master clock generator coupled to the clock bus to generate a master clock signal. This is taught as MEMORY CONTROLLER 302, SYSTEM CLOCK CIRCUIT 303, SYSTEM CLOCK BUS 348 and SYTEM CLOCK DRIVER 301, at figure 3. Johnson discloses a phase comparator having a first input coupled to the master clock generator and a second input and responsive to a phase difference between the first and second inputs to produce an adjust command, and a logic circuit. This is taught as LATCH 322, second receiver 318, SYSTEM CLOCK 348, SYSTEM CLOCK DRIVER 301, bus 320, signal lines 350, first receiver 319, output line 317, LATCH 322 and TO LOGIC CIRCUITRY, at figure 3. Johnson discloses a memory device having a clock input coupled to the clock bus, an echo signal generator to generate an echo signal responsive to the master clock signal at the clock input. This is taught as MEMORY MODULE 300, SYSTEM CLOCK CIRCUIT 303, SYSTEM CLOCK DRIVER 301, SYSTEM CLOCK 348, MEMORY MODULE 300, bus 320, bus 320, SYSTEM CLOCK 348 and SYSTEM CLOCK DRIVER

301, at figure 3. Johnson discloses the echo signal generator being coupled to the second input of the phase comparator. This is taught as memory bank **300**, bus **320**, second receiver **318** and LATCH **322**, at figure 3. Johnson discloses a data latch having a trigger input and responsive to a control signal at the trigger's input to transmit data to the data bus. This is taught as LATCH **322**, inverter **324**, READ COMMANDS **309**, inverter **324**, memory bank **300** and bus **320**, at figure 3. Johnson discloses and a variable delay circuit having a control output coupled to the trigger input and a command input coupled to the command bus. This is taught as SAMPLING CLOCK CIRCUIT **304**, DELAY MODULE **313**, inverter **324**, READ COMMANDS **309** and command bus **349**, at figure 3. Johnson discloses the delay circuit being responsive to the adjust command on the command bus to produce the control signal at a time corresponding to the adjust command. This is taught as delay module **313**, the predetermined delay, selected based upon the expected levels of memory loading, mux input lines **310**, mux driver **312** provides an output and the expected levels, at column 8 lines 1 to 32.

With respect to claim 15, Johnson discloses wherein the signal source includes a multiple output delay-locked loop. This is taught as clock signals preferably include, delayed by a different amount and the sampling clock circuit **304**, at column 7 lines 51 to 67. "The sampling clock circuit **304** continuously provides the sampling clock signals on the signal lines **350** to the clock selector **306**." "The clock signals preferably include a very early clock signal **401**, a nominal clock signal **402**, and a late clock signal **403**.

Each of these clock signals is delayed by a different amount with respect to the system clock."

With respect to claims 16 and 20, Johnson discloses a method of adjusting data timing in a memory system having a memory device and a memory controller. This is taught as coordinating access to synchronous memory, memory bank **300**, memory bank **300** and memory controller **302**, at column 5 lines 19 to 33. "The present invention generally comprises a memory controller for coordinating access to synchronous memory such as S-DRAM and S-SRAM. FIG.3 illustrates an illustrative implementation of the hardware components and interconnections of the invention, wherein a memory controller **302** manages access to a memory bank **300**."

With respect to claim 16, Johnson discloses the method comprising the steps of transmitting a first set of data, receiving the first set of data at the memory device, establishing an initial output timing, transmitting a second set of data, receiving the second set of data at the memory controller, comparing the second set of data to the first clock signal, transmitting a third set of data and revising the initial output timing. This is taught as system clock signals, system clock signals, memory bank **300**, signal indicative of the level of memory loading, Read data from the memory bank **300**, memory controller **302**, coordinate the receipt of data read, Read data from the memory bank **300**, system clock signals, provide an output signal, and signal indicative of the level of memory loading, at column 6 lines 8 to 46. Johnson discloses transmitting a first set of data to the memory device according to a first clock signal. This is taught as

provided to clock READ commands, memory bank **300** and system clock signals, at column 5 line 48 through column 6 line 7. Johnson discloses establishing an initial output timing at the memory device having a default phase relationship with the first clock signal. This is taught as signal indicative of the level of memory loading, memory bank **300**, different phase characteristics and an appropriate one of the sampling clock signals, at column 6 lines 8 to 46. Johnson discloses transmitting a second set of data from the memory device to the memory controller according to the initial output timing. This is taught as Read data from the memory bank **300**, memory bank **300**, memory controller and signal indicative of the level of memory loading, at column 6 lines 8 to 46. Johnson discloses comparing the second set of data to the first clock signal in order to identify a phase error. This is taught as Read data from the memory bank **300**, coordinate the receipt of data read from the memory bank **300** and different phase characteristics, at column 6 lines 8 to 46. Johnson discloses transmitting a third set of data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error. This is taught as provide an output signal, memory controller, memory bank **300**, signal indicative of the level of memory loading and an appropriate one of the sampling clock signals, at column 6 lines 8 to 46. Johnson discloses revising the initial output timing at the memory device according to the third set of data to produce a revised output timing. This is taught as to synchronize, compensating for data skew, signal indicative of the level of memory

loading, memory bank **300**, provide an output signal and signal indicative of the level of memory loading, at column 6 lines 8 to 46.

With respect to claim 17, Johnson discloses wherein the step of transmitting a second set of data includes transmitting an echo clock signal. This is taught as Read data from the memory bank **300** and data read from the memory bank **300**, at column 6 lines 8 to 46.

With respect to claim 18, Johnson discloses wherein the step of comparing the second set of data comprises the steps of generating a plurality of phase shifted signals, comparing the echo clock signal, identifying one of the phase shifted signals and generating a third set of data. This is taught as coordinate timing of data Read operations, sampling clock signals **400-403**, coordinate timing of data Read operations, the clock selector **306** selects one of these signals and the mux driver **312** provides its output, at column 8 lines 1 to 32. Johnson discloses generating a plurality of phase shifted signals responsive to the first clock signal. This is taught as sampling clock signals **400-403**, predetermined delay and with respect to the system clock signal, at column 8 lines 1 to 32. Johnson discloses comparing the echo clock signal to each of the phase shifted signals. This is taught as coordinate timing of data Read operations, based upon data received, clock selector **306** selects one of these signals and sampling clock signals **400-403**, at column 8 lines 1 to 32. Johnson discloses identifying one of the phase shifted signals having a phase within a selected range of phases relative to the echo clock signal. This is taught as the clock selector **306** selects one of these

signals, coordinate timing of data Read operations, sampling clock signals 400-403, spaced apart by 10 nS, coordinate timing of data Read operations and based upon data received, at column 8 lines 1 to 32. Johnson discloses generating the third set of data according to the identification of the phase shifted signal. This is taught as the mux driver 312 provides its output and the correct sampling clock signal, at column 8 lines 1 to 32.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US Patent number 5,77,236} as disclosed in claim 6 above in view of Smith et al. {US Patent number 5,020,023}. This rejection is set forth in prior Office Action, Paper No. 11.

Johnson discloses the invention substantially as claimed with claim 6. However, Johnson discloses neither the adjustment of a vernier not the use of a delay locked loop. Smith teaches the adjustment of a vernier and a phase locked loop in the analogous art of electrical computers and data processing systems for the purpose of eliminating the skew between multiple correlated synchronous data streams.

With respect to claims 7 and 19, Smith teaches wherein the step of selecting an adjusted time delay includes the step of adjusting a vernier. This is taught as automatic adjustment, frame synchronization, automatic adjustment and Vernier synchronization, at column 7 lines 16 to 21. "Since such an automatic adjustment is, in effect, adjusting for fractional frame skew, it is called Vernier synchronization. Whole frame synchronization is not required as the frame is long enough so that all elements of the system are always in whole frame synchronism with one another."

With respect to claims 12, Smith teaches wherein the signal source includes a multiple output delay-locked loop. This is taught as decode logic **30**, keyed to the waveform transitions, sync marking, frame marked bit period and phase locked loops, at column 7 lines 22 to 32. "Decode logic **30** receives the data stream and, using a phase locked loop keyed to the waveform transitions in the center of the bit period, recovers the clock. Every bit period, except the frame marked bit period, has such a transitions making the design of this phase locked loop simple. The phase locked loop parameters are selected so that the output remains stable across single bit periods without a transition. The regenerated clock makes the detection of the sync marking the frame easy."

It would have been obvious to one of ordinary skill in the art, having the teachings of Johnson and Smith before him at the time the invention was made, to modify the memory controller for reading data from synchronous RAM taught by Johnson to include the automatic vernier synchronization of skewed data streams of

Smith, because the detection of synchronization faults in a data stream while data is loading and unloading from a FIFO register. It would be advantageous to one of ordinary skill to utilize such combination because frame marked data would have been achieved as is taught by Smith. In addition, the synchronization of the receipt of data would have been achieved as is taught by both Johnson and Smith.

(11) Response to Arguments

Applicant's arguments filed 08/798,227 have been fully considered but they are not persuasive. The arguments highlight material that is already present in the prior art cited.

1. The cited art are not pertinent to the claimed inventions.

The applicant argues the Johnson et al. system does not employ "adaptive signal timing" as described above to automatically configure the memory controller and memory to optimum performance and although the multiplexer 307 can select differently phased sampling clock signals, the multiplexer 307 does not do so based on a measured timing error as in applicant's system. This is not persuasive because Johnson discloses this with the clock selector **306** that chooses the clock signal **402** from a variety of clock signals as the default, in order to introduce a greater delay in delay module **313**, at column 9 lines 19 to 27. "With a larger data skew, for example, a clock signal on one of the signal lines **350** would be chosen to introduce a greater delay into the delay module **313**. After the memory modules **300*a*-300*d*** receive a Read

command from the command bus **349**, the memory modules **300*a*-300*d*** place the requested data on the bus **320**. In an exemplary embodiment of the invention, the clock selector **306** chooses the clock signal **402** as a default if no other clock signal **400-401** or **403** is selected."

The Applicant argues the adjustment made by the multiplexer 307 is performed in the memory controller rather than in the memory devices. The argument is not persuasive because Johnson discloses this with a clock sampling circuit **304** which feeds the multiplexer **307** for selecting the sampling clock signal within the memory controller **302**, rather than the memory devices **300**, at figure 3 and column 6 lines 8 to 18. "The memory controller also includes a sampling clock circuit **304** to coordinate the receipt of data read from the memory bank **300** during the appropriate data valid window, thus compensating for data skew. In particular, one of the sampling clock signals from the sampling clock circuit **304** is selectively fed to a delay module **313**, which provides a delayed clock signal to a first receiver **319** via an output line **317**, to synchronize the receipt by a latch **322** of Read data from the memory bank **300** during the appropriate data valid window."

Thus the Johnson et al. patent does not disclose a structure or operation where the memory controller 302 identifies a phase error between a signal transmitted from the memory device and a clock signal of the memory controller 302, and then transmits data to the memory bank 300 in order to cause the memory bank 300 to revise the timing at which it outputs data. The argument is not persuasive because Johnson

discloses this with the memory controller also includes a clock sampling circuit **304** used to coordinate the receipt of data read from the memory bank **300**, at column 6 lines 8 to 18.

2. The Claims Represented by Independent Claim 20 Patentably Distinguish over the Cited References.

The Applicant argues the Johnson et al. patent does not disclose a memory controller that identifies a phase error between a received digital signal relative to a timing reference signal, nor does the system transmit an adjustment signal to the memory device to cause the memory device to revise the initial output timing. This is not persuasive because Johnson discloses this with the memory controller also includes a clock sampling circuit **304** coordinated with the receipt of data read from the memory bank **300** compensating for data skew to synchronize the receipt by a latch **322**, at column 6 lines 8 to 18.

The Applicant argues the Johnson et al. patent does not disclose any system in which the timing of a signal generated by a memory device can be adjusted. This is not persuasive because Johnson discloses this with a clock signal on one of the signal lines **350** would be chosen to introduce a greater delay into the delay module **313**, at column 9 lines 19 to 27.

Smiths use of "vernier" has nothing to do with disclosing or suggesting adjusting a vernier in adjusting a time delay in response to the relative phase relationship between two signals. Smith's reference to "vernier" simply describes making

adjustments in less than whole increments. This is not persuasive because Smith discloses this with adjusting for fractional frame skew called Vernier synchronization to eliminate the necessity of a whole frame synchronization, at column 7 lines 16 to 32 and column 10 lines 39 to 49. "Since such an automatic adjustment is, in effect, adjusting for fractional frame skew, it is called Vernier synchronization. Whole frame synchronization is not required as the frame is long enough so that all elements of the system are always in whole frame synchronism with one another." "FIG. 6 shows and implementation of the procedure illustrated in the flow diagram of FIG. 5. Decode logic **30** receives the data stream and, using a phase locked loop keyed to the waveform transitions in the center of the bit period, recovers the clock. Every bit period, except the frame marked bit period, has such a transitions making the design of this phase locked loop simple. The phase locked loop parameters are selected so that the output remains stable across single bit periods without a transition. The regenerated clock makes the detection of the sync marking the frame easy." "In FIG. 9A, the channel head **70** receives the data stream and replicates the data stream to each of the triplex channel repeaters **71**, **73** and **75**. The outputs of the triplex channel repeaters are supplied to each of three triplex channel voters as the input to a channel engine **72**, **74** and **76** (only one of which is shown for the sake of simplicity). Each triplexed front-end component, i.e., channel repeater and channel voter, accepts the incoming data stream from the channel head **70**, performing the necessary skew compensation using Vernier Skew compensation as described above." The use of a phase locked loop delay

module creates a vernier skew, which delays signals only a part of the time for a frame. In this manner, synchronization of a signal does not require holding back the clock signal until the signal has made its way through the entire system as a whole frame synchronization will require. By making the delay of the delay locked loop long enough, whole frame synchronization may be mimicked or even exceeded.

3. The Claims Represented by Independent Claim 21 Patentably Distinguish over the Cited References.

The Applicant argues the only "plurality of phase shifted signals" disclosed in the Johnson et al. patent are the sampling clock signals generated by the sampling clock circuit 304. This is not persuasive because Johnson discloses this with a primary system clock **348** bypassing the sampling clock circuit **304**, passing through the system clock driver **301** and the memory module **300** to be captured by the latch **322** for comparison by the logic circuitry for identifying the proper state of that latch **322**, at figure 3.

4. The Claims Represented by Independent Claim 10 Patentably Distinguish over the Cited References.

The Applicant argues the Johnson system does not have a phase comparing circuit which compares the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. This is not persuasive because Johnson discloses this with the output of a clock selector **306** coordinating timing of the data read operations with the memory bank **300** causing the mux **307** to

provide the desired sampling signal, at column 8 lines 23 to 32. "Generally, the clock selector **306** selects one of these signals to forward to the delay module **313**, to coordinate timing of data Read operations with the memory bank **300**. More specifically, the mux driver **312** provides an output on the mux input lines **310**, causing the mux **307** to output the correct sampling clock signal on the signal line **352**. In an illustrative embodiment, the mux driver **312** provides its output based upon data received from a data source **305** via a selector bus **311**, in the manner discussed below."

5. The Claims Represented by Independent Claim 11 Patentably Distinguish over the Cited References.

As explained above in section 3, the only "plurality of phase shifted signals" disclosed in the Johnson et al. patent are the sampling clock signals, which are not compared to any other signals. This is not persuasive because Johnson discloses this with clock selector **306** selects one of these signals to coordinate timing of the memory bank **300**, at column 8 lines 23 to 32.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

David Ransom

Examiner: David Ransom

Conferee: Behzad James Peikari

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